memory means connected to each of said compressing means and said generating means and having a common memory for storing the video signal to perform a compressing process by said compressing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 33. (Amended) An apparatus according the claim 29, further comprising:

reproducing means for reproducing from the recording medium the video signal the amount of which has been compressed by said compressing means, and for writing the reproduced video signal into said memory means. --.

– 34. (Amended) An apparatus according to claim 33, further comprising:

expanding means for expanding an amountof information of the reproduced video signal by using said memory means; and

combining means for combining the character siganl with the video signal the amount of which has been expanded by said expanding means. –.

REMARKS

Claims 1, 7, 9, 12, 16-18, 20, 22, 24, 26, 28, 29, 33 and 34 have been amended. Attached hereto is a marked-up version of the changes made to the claims by this Amendment. This marked-up version has been entitled "Version With Markings To Show Changes Made."

Claims 1-6, 12-16, 20 and 29-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata patent taken in view of Parulski et al. and Jeong patents. The remaining dependent claims have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the latter three patents taken in further view of one or more of the Ota, Honda and Yonemitsu

et al. patents. With respect to applicant's claims, as amended, these rejections are respectfully traversed.

Independent claims 1, 12, 20 and 29 have each been amended to better define applicant's invention. In particular, these claims recite a memory means having a common memory for storing the video signal to perform either a compressing, expanding or other predetermined process by a respective compressing, expanding or processing means and storing the character signal generated by a generating means to perform a combining operation of the character signal. Additionally, the claims now further recite that the memory means is connected to the respective compressing, expanding or processing means and to the generating means. The cited patents are not believed to teach or suggest this construction.

The Yamagata patent discloses the feature of storing image data picked up by a CCD in an image memory (35) and the structure of a compression/expansion circuit (44) for compressing or expanding the image data. Yamagata also discloses that image data read from the image memory (35) is stored in the IC memory card (M) and that a non-compression mode, a low compression mode, and a high compression mode can be selected with respect to the image data stored in the IC memory card (M).

As the Examiner has pointed out, however, the Yamagata reference fails to teach or suggest a generating means for generating a character signal, or that the memory used for image processing, such as compression or expansion of the image signal, is also used for such character signal generation. Moreover, this patent does not teach or suggest that the generating means and the expansion, compressing or expanding means be connected to a common memory.

The Parulski et al. reference discloses an image buffer (18) storing therein one or more still images, a processor (20) for controlling the image buffer, a date and time generator (20a) which supplies date and time information to the processor (20), a processor (22) for compressing the images using an algorithm such as JPEG, which algorithms are stored in memory (28), and the storage of such compressed image in the memory card (24). However, while the memory card (24) contains additional memory to store header files (24b) for "tagging" the already processed images with character strings, it cannot be said that the device of Parulski et al. uses the same memory for processing (e.g., compressing or expanding) image information as it does for generating character information.

Thus, the Parulski et al. patent fails to teach or suggest that the memory used for image processing, such as compression or expansion of the still image, is also used for generating a character signal or that the processing, expansion or compression means and the generating means are connected to such memory.

The Examiner recognizing the failings of the Yamagata and Parulski, et al. patents in teaching or suggestion applicant's invention, now cites the Jeong patent with these patents and argues as follows:

> "Jeong teaches partitioning a single memory into several parts in figure 3. It would have been obvious to partition a memory mean to allow the memory to be used in a compression process and a character generation combining process.
>
> It would have been highly desirable to have a generating means so that the users could add text to the images. It would have been highly desirable to partition the memory to allow compression and character generation to be done using a single memory thereby reducing the number of parts needed for the device.

Therefor, it would have been obvious to a person of ordinary skill in the art at the time of the invention have a character generator and a video signal in Yamagata."

The Examiner's reasoning, however, fails to consider the totality of the teachings of the Jeong patent. Jeong teaches dividing a memory 234 into three areas, an EFM demodulation and ECC decoding area, a track buffer area and a micron memory area and using the three areas. However, the memory in the Jeong patent does not store a character signal. In the patent, a character signal (OSD data) is generated in an OSD controller 270, whose structure is unrelated to the memory 324. Thus, the Jeong patent also fails to teach or suggest that a memory be used for image processing, such as compression or expansion of an image, and also for generating a character signal.

Additionally, in the Jeong patent, only a data processor 230 is connected to the memory 234. Thus, the Jeong patent likewise fails to teach or suggest that a memory used for image processing and for generating a character signal, also be connected to the processing means and the generating means.

The structure of the subject invention permits signals from different sources, such as a video signal and a character signal, to be connected to a memory device which includes a common memory so as to prevent dispersion of work memory. In addition by connecting a processing circuit (e.g., compressing circuit or/and expanding circuit) and a character generating circuit that use a common memory to the common memory, respectively, circuits are able to be structured centered around the common memory so as to produce beneficial effects such as improving the processing speed and inhibiting an increase in circuit scale.

The cited Yamagata, Parulski, et al. and Jeong patents, individually, and, in combination, as set forth above, simply do not teach or suggest such a construction. Applicant's amended independent claims 1, 12, 20 and 29, and their respective dependent claims, thus patentably distinguish over these patents. Additionally, the other cited patents, Ota, Honda and Yonemitsu et al., fail to add anything to change this conclusion.

In view of the above, it is submitted that applicant's claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

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Respectfully submitted,

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Version With Markings To Show Changes Made

In the Claims

Amend claims 1, 7, 9, 12, 16-18, 20, 22, 24, 26, 28, 29 and 33-34 as follows:

-- 1. (Twice Amended) A signal processing device, comprising:

inputting means for inputting a video signal;

compressing means for compressing an amount of information of the video signal;

generating means for generating a character signal; and

memory means connected to each of said compressing means and said generating means and having a common memory for storing the video signal to perform a compressing process by said compressing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 7. (Amended) A device according to claim 1, wherein said memory means has a first area for storing a video signal an amount of which is to be compressed by said compressing means, a second area for storing a video signal an amount of which has been compressed by said compressing means, and a third area which is different from said first area and said second area, said generating means generating the character signal by using the third area --.

-- 9. (Amended) A device according to claim 1, wherein said memory means has a first area which is to be accessed by said compressing means, and a second area which corresponds to an image plane represented by the video signal and which is different from the first area, and wherein said generating means comprises memory control means for writing into said second area a plurality of codes representing a value of pixel data of the character signal, and a table

for outputting pixel data corresponding to codes read out from said second area. --.

-- 12. (Twice Amended) A signal processing device, comprising:

inputting means for inputting a video signal;

expanding means for expanding an amount of information of the video signal;

generating means for generating a character signal; and

memory means connected to each of said compressing means and said generating means and having a common memory for storing the video signal to perform an expanding process by said expanding means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 16. (Amended) A device according to claim 12, [further comprising:] wherein said inputting means for inputting [a] the video signal reproduced from a recording medium by a reproduction device and writing the reproduced video signal into said memory means, said expanding means expanding an amount of information of the video signal written into said memory means by said inputting means. --.

-- 17. (Amended) A device according to claim 12, wherein said memory means has a first area for storing a video signal an amount of which is to be expanded by said expanding means, a second area for storing a video signal an amount of which has been expanded by said expanding means, and a third area which is different from said first area and said second area, said [expanding] generating means generating the third character signal by using said third area. --.

-- 18. (Twice Amended) A device according to claim 12, wherein said memory means has a first area which is to be accessed by said expanding means, and a second area which corresponds to an image plane represented by the video signal and which is different from said first area, and

wherein said generating means comprises memory control means for writing into said second area a plurality of codes representing a value of pixel data of the character signal, and a table for outputting pixel data corresponding to codes read out from said second area.

-- 20. (Twice Amended) A signal processing device, comprising:

inputting means for inputting a video signal;

processing means for performing a predetermined process on the video signal;

generating means for generating a character signal; and

memory means connected to each of said compressing means and said generating means and having a common memory for storing the video signal to perform the predetermined process by said processing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 22. (Amended) A device according to claim 21, wherein said memory means has a first area which is to be accessed by said high-efficiency encoding means, and a second area other than said first area, said generating means generating the character signal by using the second area. --.

-- 24. (Amended) A device according to claim 23, wherein said memory means has a first area which is to be accessed by said high-efficiency encoding means, a second area which is to be accessed by said error correction encoding means, and a third area other than said first area and said second area, said generating means generating the character signal using said third area. --.

-- 26. (Amended) A device according to claim 25, wherein said memory means has a first area which is to be accessed by said high-efficiency decoding means, and a second area other than said first area, said generating means generating the character signal by using said second area. --.

-- 28. (Amended) A device according to claim 27, wherein said memory means includes a first area which is to be accessed by said high-efficiency decoding means, a second area which is to be accessed by said error correction decoding means, and a third area other than said first area and said second area, said generating means generating the character signal by using said third area. --.

-- 29. (Twice Amended) A recording apparatus, comprising:

inputting means for inputting a video signal;

compressing means for compressing an amount of information of the video signal;

recording means for recording on a recording medium the video signal the amount of which has been compressed by said compressing means;

generating means for generating a character signal; and

memory means connected to each of said compressing means and said generating means and having a common memory for storing the video signal to perform a compressing process by said compressing means and storing the character signal generated by said generating means to perform a combining operation of the character signal. --.

-- 33. (Amended) An apparatus according the claim 29, further comprising:

reproducing means for reproducing from the recording medium the video signal the amount of which has been compressed by said compressing means, and for writing the reproduced video signal into said memory means. --.

-- 34. (Amended) An apparatus according to claim 33, further comprising:

expanding means for expanding an amountof information of the reproduced video signal by using said memory means; and

combining means for combining the character siganl with the video signal the amount of which has been expanded by said expanding means. --.